

**SN5412, SN54LS12  
SN7412, SN74LS12**

SDLS040

**TRIPLE 3-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS**

DECEMBER 1983—REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

**description**

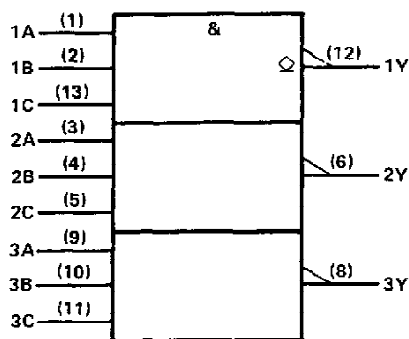
These devices contain three independent 3-input NAND gates with open-collector outputs. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher  $V_{OH}$  levels.

The SN5412 and SN54LS12 are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN7412 and SN74LS12 are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

**FUNCTION TABLE (each gate)**

INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

**logic symbol†**

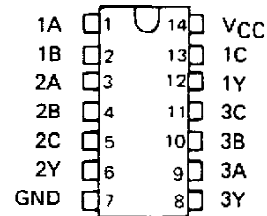


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

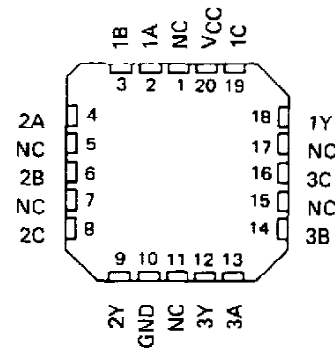
SN5412, SN54LS12 . . . J OR W PACKAGE  
SN7412 . . . N PACKAGE  
SN74LS12 . . . D OR N PACKAGE

(TOP VIEW)



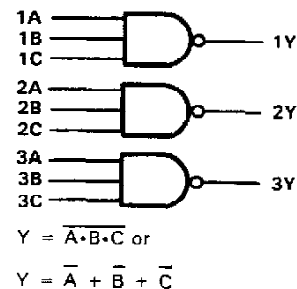
SN54LS12 . . . FK PACKAGE

(TOP VIEW)



NC—No internal connection

**logic diagram (positive logic)**



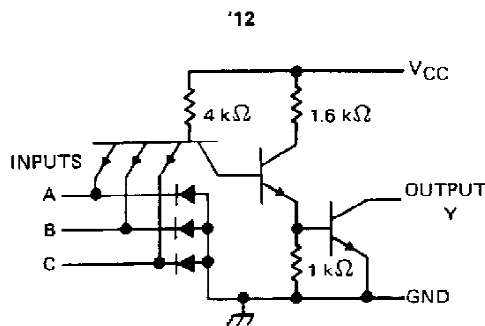
PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



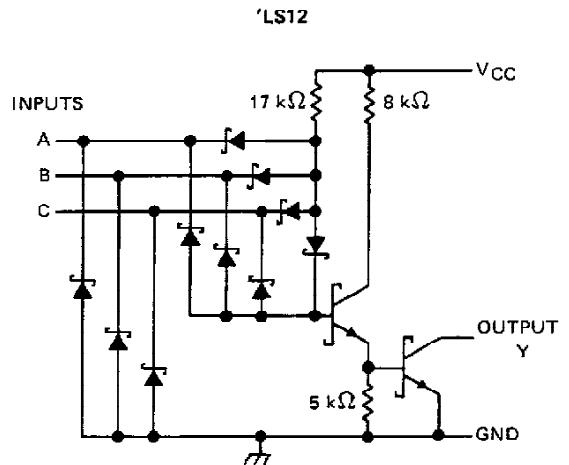
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**SN5412, SN54LS12  
SN7412, SN74LS12  
TRIPLE 3-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS**

schematics (each gate)



Resistor values shown are nominal.



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage: '12	5.5 V
'LS12	7 V
Off-state output voltage	7 V
Operating free-air temperature: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

# SN5412, SN5412

## TRIPLE 3-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

### recommended operating conditions

	SN5412			SN7412			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub> Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub> High-level input voltage	2			2			V
V <sub>IL</sub> Low-level input voltage			0.8			0.8	V
V <sub>OH</sub> High-level output voltage			5.5			5.5	V
I <sub>OL</sub> Low-level output current			16			16	mA
T <sub>A</sub> Operating free-air temperature	-55		125	0		70	°C

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN5412			SN7412			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = MIN, I <sub>I</sub> = -12 mA			-1.5			-1.5	V
I <sub>OH</sub>	V <sub>CC</sub> = MIN, V <sub>IL</sub> = 0.8 V, V <sub>OH</sub> = 5.5 V						0.25	mA
	V <sub>CC</sub> = MIN, V <sub>IL</sub> = 0.7 V, V <sub>OH</sub> = 5.5 V			0.25				
V <sub>OL</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 16 mA		0.2	0.4		0.2	0.4	V
I <sub>I</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V			1			1	mA
I <sub>IH</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.4 V			40			40	μA
I <sub>IL</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V			-1.6			-1.6	mA
I <sub>CCH</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0		3	6		3	6	mA
I <sub>CCL</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 4.5 V		9	16.5		9	16.5	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

### switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	A, B or C	Y	R <sub>L</sub> = 4 kΩ,	C <sub>L</sub> = 15 pF		35	45	ns
t <sub>PHL</sub>			R <sub>L</sub> = 400 Ω,	C <sub>L</sub> = 15 pF		8	15	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

  
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# SN54LS12, SN74LS12

## TRIPLE 3-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

### recommended operating conditions

	SN54LS12			SN74LS12			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub> Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub> High-level input voltage	2			2			V
V <sub>IL</sub> Low-level input voltage			0.7			0.8	V
V <sub>OH</sub> High-level output voltage			5.5			5.5	V
I <sub>OL</sub> Low-level output current			4			8	mA
T <sub>A</sub> Operating free-air temperature	-55		125	0		70	°C

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54LS12			SN74LS12			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA		-1.5			-1.5	V	
I <sub>OH</sub>	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>OH</sub> = 5.5 V		0.1			0.1	mA	
V <sub>OL</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 4 mA		0.25	0.4		0.25	0.4	V
	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 8 mA					0.35	0.5	
I <sub>I</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V		0.1			0.1	mA	
I <sub>IH</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V		20			20	μA	
I <sub>IL</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V		-0.4			-0.4	mA	
I <sub>CC</sub> H	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0		0.7	1.4		0.7	1.4	mA
I <sub>CC</sub> L	V <sub>CC</sub> = MAX, V <sub>I</sub> = 4.5 V		1.8	3.3		1.8	3.3	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

### switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	A, B or C	Y	R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 15 pF		17	32	ns
t <sub>PHL</sub>					15	28	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

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