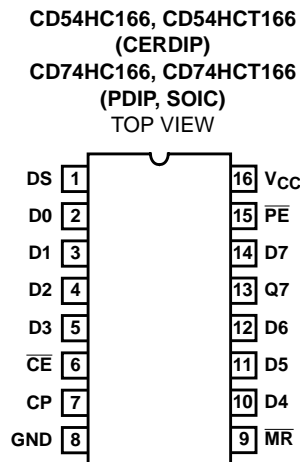


## High-Speed CMOS Logic 8-Bit Parallel-In/Serial-Out Shift Register

### Features

- Buffered Inputs
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5V$
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8V$  (Max),  $V_{IH} = 2V$  (Min)

### Pinout



### Description

The 'HC166 and 'HCT166 8-bit shift register is fabricated with silicon gate CMOS technology. It possesses the low power consumption of standard CMOS integrated circuits, and can operate at speeds comparable to the equivalent low power Schottky device.

The 'HCT166 is functionally and pin compatible with the standard 'LS166.

The 166 is an 8-bit shift register that has fully synchronous serial or parallel data entry selected by an active LOW Parallel Enable (PE) input. When the PE is LOW one setup time before the LOW-to-HIGH clock transition, parallel data is entered into the register. When PE is HIGH, data is entered into the internal bit position Q0 from Serial Data Input (DS), and the remaining bits are shifted one place to the right (Q0 → Q1 → Q2, etc.) with each positive-going clock transition. For expansion of the register in parallel to serial converters, the Q7 output is connected to the DS input of the succeeding stage.

The clock input is a gated OR structure which allows one input to be used as an active LOW Clock Enable (CE) input. The pin assignment for the CP and CE inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of CE input should only take place while the CP is HIGH for predictable operation.

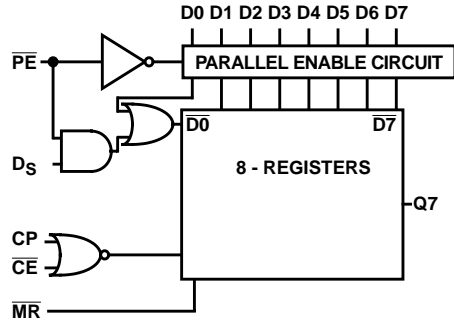
A LOW on the Master Reset (MR) input overrides all other inputs and clears the register asynchronously, forcing all bit positions to a LOW state.

### Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC166F3A	-55 to 125	16 Ld CERDIP
CD54HCT166F3A	-55 to 125	16 Ld CERDIP
CD74HC166E	-55 to 125	16 Ld PDIP
CD74HC166M	-55 to 125	16 Ld SOIC
CD74HC166MT	-55 to 125	16 Ld SOIC
CD74HC166M96	-55 to 125	16 Ld SOIC
CD74HCT166E	-55 to 125	16 Ld PDIP
CD74HCT166M	-55 to 125	16 Ld SOIC
CD74HCT166MT	-55 to 125	16 Ld SOIC
CD74HCT166M96	-55 to 125	16 Ld SOIC

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

**Functional Diagram**



**TRUTH TABLE**

INPUTS						INTERNAL Q STATES		OUTPUT Q7
MASTER RESET	PARALLEL ENABLE	CLOCK ENABLE	CLOCK	SERIAL	PARALLEL	Q0	Q1	
					D0 D7			
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q00	Q10	Q0
H	L	L	↑	X	a...h	a	b	h
H	H	L	↑	H	X	H	Q0n	Q6n
H	H	L	↑	L	X	L	Q0n	Q6n
H	X	H	↑	X	X	Q00	Q10	Q70

H= High Voltage Level

L= Low Voltage Level

X= Don't Care

↑= Transition from Low to High Level

a...h = The level of steady-state input at inputs D0 thru D7, respectively.

Q00, Q10, Q70 = The level of Q0, Q1, or Q7, respectively, before the indicated steady-state input conditions were established.

Q0n, Q6n = The level of Q0 or Q6, respectively, before the most recent ↑ transition of the clock.

# CD54HC166, CD74HC166, CD54HCT166, CD74HCT166

## Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ .....	-0.5V to 7V
DC Input Diode Current, $I_{IK}$	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Output Diode Current, $I_{OK}$	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Drain Current, per Output, $I_O$	
For $-0.5V < V_O < V_{CC} + 0.5V$ .....	$\pm 25mA$
DC Output Source or Sink Current per Output Pin, $I_O$	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ .....	$\pm 25mA$
DC $V_{CC}$ or Ground Current, $I_{CC}$ or $I_{GND}$ .....	$\pm 50mA$

## Thermal Information

Thermal Resistance (Typical, Note 1)	$\theta_{JA}$ (°C/W)
E (PDIP) Package .....	67
M (SOIC) Package .....	73
Maximum Junction Temperature .....	150°C
Maximum Storage Temperature Range .....	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s) .....	300°C (SOIC - Lead Tips Only)

## Operating Conditions

Temperature Range ( $T_A$ ) .....	-55°C to 125°C
Supply Voltage Range, $V_{CC}$	
HC Types .....	.2V to 6V
HCT Types .....	4.5V to 5.5V
DC Input or Output Voltage, $V_I, V_O$ .....	0V to $V_{CC}$
Input Rise and Fall Time	
2V .....	1000ns (Max)
4.5V .....	500ns (Max)
6V .....	400ns (Max)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

### NOTE:

- The package thermal impedance is calculated in accordance with JESD 51-7.

## DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		$V_{CC}$ (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		$V_I$ (V)	$I_O$ (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>												
High Level Input Voltage	$V_{IH}$	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	$V_{IL}$	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	$I_I$	$V_{CC}$ or GND	-	6	-	-	$\pm 0.1$	-	$\pm 1$	-	$\pm 1$	$\mu A$

**CD54HC166, CD74HC166, CD54HCT166, CD74HCT166**

**DC Electrical Specifications (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Quiescent Device Current	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	6	-	-	8	-	80	-	160	μA
<b>HCT TYPES</b>												
High Level Input Voltage	V <sub>IH</sub>	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V <sub>IL</sub>	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> to GND	0	5.5	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	-	-	8	-	80	-	160	μA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI <sub>CC</sub> (Note 2)	V <sub>CC</sub> -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

NOTE:

- For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4V, V<sub>CC</sub> = 5.5V) specification is 1.8mA.

**HCT Input Loading Table**

INPUT	UNIT LOADS
DS, D0-D7	0.2
PE	0.35
CP, CE	0.5
MR	0.2

NOTE: Unit Load is ΔI<sub>CC</sub> limit specified in DC Electrical Specifications table, e.g., 360μA max at 25°C.

**Prerequisite For Switching Specifications**

PARAMETER	SYMBOL	V <sub>CC</sub> (V)	25°C		-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>									
Clock Frequency (Figure 1)	f <sub>MAX</sub>	2	6	-	5	-	4	-	MHz
		4.5	30	-	25	-	20	-	MHz
		6	35	-	29	-	23	-	MHz

**CD54HC166, CD74HC166, CD54HCT166, CD74HCT166**

**Prerequisite For Switching Specifications (Continued)**

PARAMETER	SYMBOL	V <sub>CC</sub> (V)	25°C		-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
$\overline{MR}$ Pulse Width (Figure 1)	t <sub>w</sub>	2	100	-	125	-	150	-	ns
		4.5	20	-	25	-	30	-	ns
		6	17	-	21	-	26	-	ns
Clock Pulse Width (Figure 1)	t <sub>w</sub>	2	80	-	100	-	120	-	ns
		4.5	16	-	20	-	24	-	ns
		6	14	-	17	-	20	-	ns
Set-up Time Data and $\overline{CE}$ to Clock (Figure 5)	t <sub>SU</sub>	2	80	-	100	-	120	-	ns
		4.5	16	-	20	-	24	-	ns
		6	14	-	17	-	20	-	ns
Hold Time Data to Clock (Figure 5)	t <sub>H</sub>	2	1	-	1	-	1	-	ns
		4.5	1	-	1	-	1	-	ns
		6	1	-	1	-	1	-	ns
Removal Time $\overline{MR}$ to Clock (Figure 5)	t <sub>REM</sub>	2	0	-	0	-	0	-	ns
		4.5	0	-	0	-	0	-	ns
		6	0	-	0	-	0	-	ns
Set-up Time $\overline{PE}$ to CP (Figure 5)	t <sub>SU</sub>	2	145	-	180	-	220	-	ns
		4.5	29	-	36	-	44	-	ns
		6	25	-	31	-	38	-	ns
Hold Time $\overline{PE}$ to CP or $\overline{CE}$ (Figure 5)	t <sub>H</sub>	2	0	-	0	-	0	-	ns
		4.5	0	-	0	-	0	-	ns
		6	0	-	0	-	0	-	ns
<b>HCT TYPES</b>									
Clock Frequency (Figure 2)	f <sub>MAX</sub>	4.5	25	-	20	-	16	-	MHz
$\overline{MR}$ Pulse Width (Figure 2)	t <sub>w</sub>	4.5	35	-	44	-	53	-	ns
Clock Pulse Width (Figure 2)	t <sub>w</sub>	4.5	20	-	25	-	30	-	ns
Set-up Time Data and $\overline{CE}$ to Clock (Figure 6)	t <sub>SU</sub>	4.5	16	-	20	-	24	-	ns
Hold Time Data to Clock (Figure 6)	t <sub>H</sub>	4.5	0	-	0	-	0	-	ns
Removal Time $\overline{MR}$ to Clock (Figure 6)	t <sub>REM</sub>	4.5	0	-	0	-	0	-	ns
Set-up Time $\overline{PE}$ to CP (Figure 6)	t <sub>SU</sub>	4.5	30	-	38	-	45	-	ns
Hold Time $\overline{PE}$ to CP or $\overline{CE}$ (Figure 6)	t <sub>H</sub>	4.5	0	-	0	-	0	-	ns

**Switching Specifications** Input t<sub>r</sub>, t<sub>f</sub> = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V <sub>CC</sub> (V)	25°C		-40°C TO 85°C	-55°C TO 125°C	UNITS
				TYP	MAX	MAX	MAX	
<b>HC TYPES</b>								
Propagation Delay, Clock to Output (Figure 3)	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	160	200	240	ns
			4.5	-	32	40	48	ns
		C <sub>L</sub> = 15pF	5	13	-	-	-	ns
			6	-	27	34	41	ns

## CD54HC166, CD74HC166, CD54HCT166, CD74HCT166

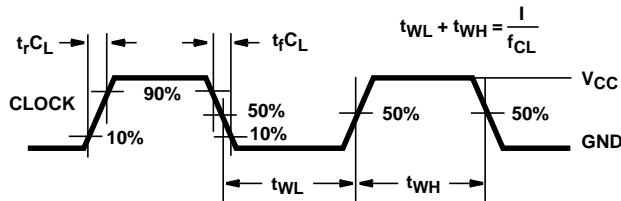
### Switching Specifications Input $t_r, t_f = 6\text{ns}$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	$V_{CC}$ (V)	25°C		-40°C TO 85°C	-55°C TO 125°C	UNITS
				TYP	MAX	MAX	MAX	
Output Transition Time (Figure 3)	$t_{TLH}, t_{THL}$	$C_L = 50\text{pF}$	2	-	75	95	110	ns
			4.5	-	15	19	22	ns
			6	-	13	16	19	ns
Propagation Delay MR to Output (Figure 3)	$t_{PHL}$	$C_L = 50\text{pF}$	2	-	160	200	240	ns
			4.5	-	32	40	48	ns
			6	-	27	34	41	ns
Input Capacitance	$C_I$	-	-	-	10	10	10	pF
Power Dissipation Capacitance (Notes 3, 4)	$C_{PD}$	-	5	41	-	-	-	pF
<b>HCT TYPES</b>								
Propagation Delay, Clock to Output (Figure 4)	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	40	50	60	ns
Output Transition Time (Figure 4)	$t_{TLH}, t_{THL}$	$C_L = 50\text{pF}$	4.5	-	15	19	22	ns
Propagation Delay MR to Output (Figure 4)	$t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	40	50	60	ns
Input Capacitance	$C_I$	-	-	-	10	10	10	pF

**NOTES:**

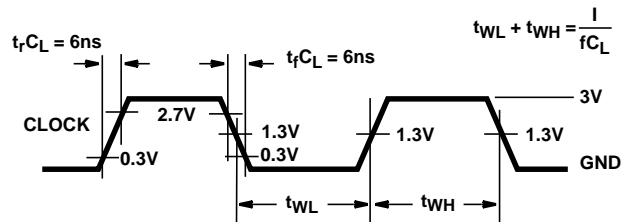
- $C_{PD}$  is used to determine the dynamic power consumption, per gate.
- $P_D = C_{PD} V_{CC}^2 f_i + \sum (C_L V_{CC}^2 + f_o)$  where  $f_i$  = Input Frequency,  $f_o$  = Output Frequency,  $C_L$  = Output Load Capacitance,  $V_{CC}$  = Supply Voltage.

### Test Circuits and Waveforms



NOTE: Outputs should be switching from 10%  $V_{CC}$  to 90%  $V_{CC}$  in accordance with device truth table. For  $f_{MAX}$ , input duty cycle = 50%.

**FIGURE 1. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH**



NOTE: Outputs should be switching from 10%  $V_{CC}$  to 90%  $V_{CC}$  in accordance with device truth table. For  $f_{MAX}$ , input duty cycle = 50%.

**FIGURE 2. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH**

Test Circuits and Waveforms (Continued)



FIGURE 3. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

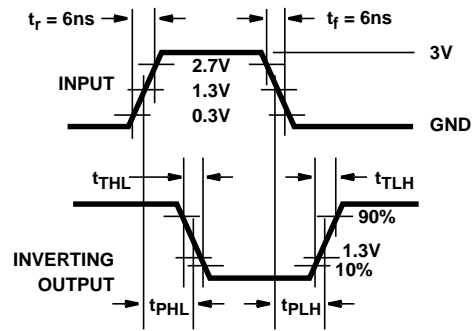


FIGURE 4. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

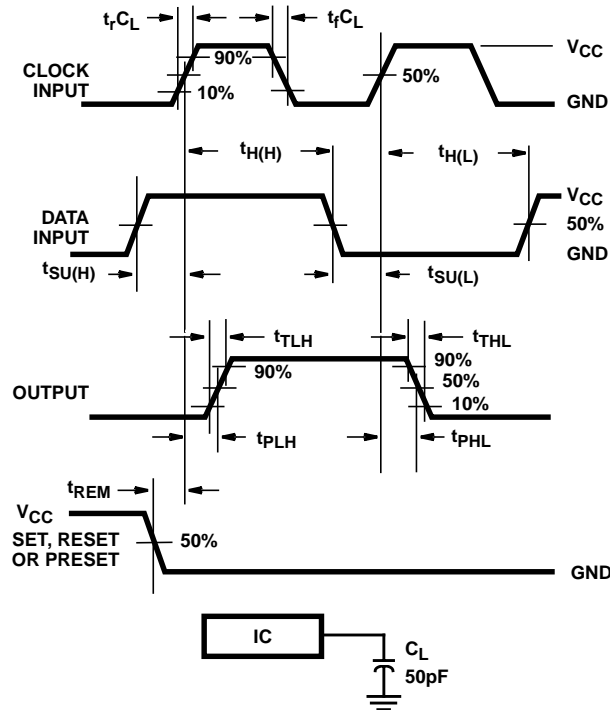


FIGURE 5. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

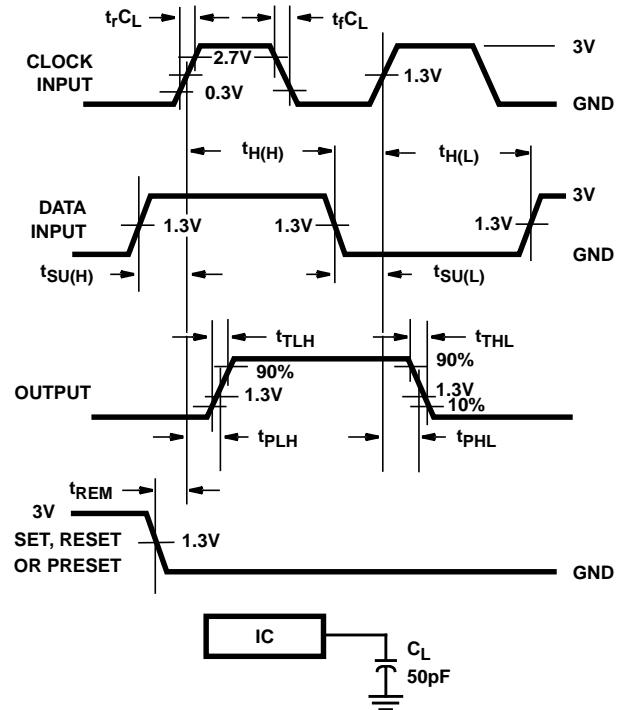


FIGURE 6. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS