

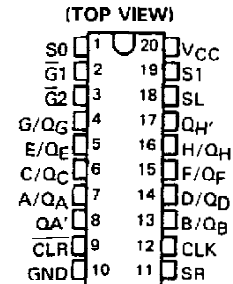
# SN54LS323, SN74LS323 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

SDLS160

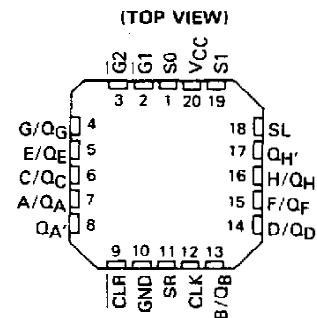
OCTOBER 1976 — REVISED MARCH 1988

- Multiplexed Inputs/Outputs Provide Improved Bit Density
- Four Modes of Operation:
  - Hold (Store)    Shift Left
  - Shift Right    Load Data
- Operates with Outputs Enabled or at High Z
- 3-State Outputs Drive Bus Lines Directly
- Can Be Cascaded for N-Bit Word Lengths
- Typical Power Dissipation . . . 175 mW
- Exceptionally Stable Shift (Clock) Frequency . . . 25 MHz
- Applications:
  - Stacked or Push-Down Registers, Buffer Storage, and Accumulator Registers
- SN54LS299 and SN74LS299 Are Similar But Have Direct Overriding Clear

SN54LS323 . . . J OR W PACKAGE  
SN74LS323 . . . DW OR N PACKAGE



SN54LS323 . . . FK PACKAGE



## description

These Low-Power Schottky eight-bit universal registers feature multiplexed inputs/outputs to achieve full eight-bit data handling in a single 20-pin package. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table. Synchronous parallel loading is accomplished by taking both function-select lines, S0 and S1, high. This places the three-state outputs in a high-impedance state, which permits data that is applied on the input/output lines to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. The clear function is synchronous, and a low level at the clear input clears the register on the next low-to-high transition of the clock.

FUNCTION TABLE

MODE	INPUTS				INPUTS/OUTPUTS								OUTPUTS					
	CLR	FUNCTION SELECT		OUTPUT CONTROL	CLK	SERIAL		A/QA	B/QB	C/QC	D/QD	E/QE	F/QF	G/QG	H/QH	QA'	QH'	
		S1	S0	G1†		G2†	SL											SR
Clear	L	X	L	L	L	†	X	X	L	L	L	L	L	L	L	L	L	
	L	L	X	L	L	†	X	X	L	L	L	L	L	L	L	L	L	
	L	H	H	X	X	†	X	X	X	X	X	X	X	X	X	X	X	
Hold	H	L	L	L	L	X	X	X	QA0	QB0	QC0	QD0	QE0	QF0	QG0	QH0	QA0	QH0
	H	X	X	L	L	L	X	X	QA0	QB0	QC0	QD0	QE0	QF0	QG0	QH0	QA0	QH0
Shift Right	H	L	H	L	L	†	X	H	H	QA <sub>n</sub>	QB <sub>n</sub>	QC <sub>n</sub>	QD <sub>n</sub>	QE <sub>n</sub>	QF <sub>n</sub>	QG <sub>n</sub>	H	QH <sub>n</sub>
	H	L	H	L	L	†	X	L	L	QA <sub>n</sub>	QB <sub>n</sub>	QC <sub>n</sub>	QD <sub>n</sub>	QE <sub>n</sub>	QF <sub>n</sub>	QG <sub>n</sub>	L	QH <sub>n</sub>
Shift Left	H	H	L	L	L	†	H	X	QB <sub>n</sub>	QC <sub>n</sub>	QD <sub>n</sub>	QE <sub>n</sub>	QF <sub>n</sub>	QG <sub>n</sub>	QH <sub>n</sub>	H	QA <sub>n</sub>	H
	H	H	L	L	L	†	L	X	QB <sub>n</sub>	QC <sub>n</sub>	QD <sub>n</sub>	QE <sub>n</sub>	QF <sub>n</sub>	QG <sub>n</sub>	QH <sub>n</sub>	L	QA <sub>n</sub>	L
Load	H	H	H	X	X	†	X	X	a	b	c	d	e	f	g	h	a	h

†When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

a . . . h = the level of the steady-state input at inputs A through H, respectively. These data are loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals.

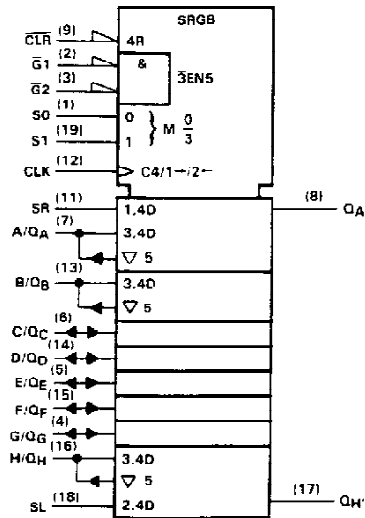
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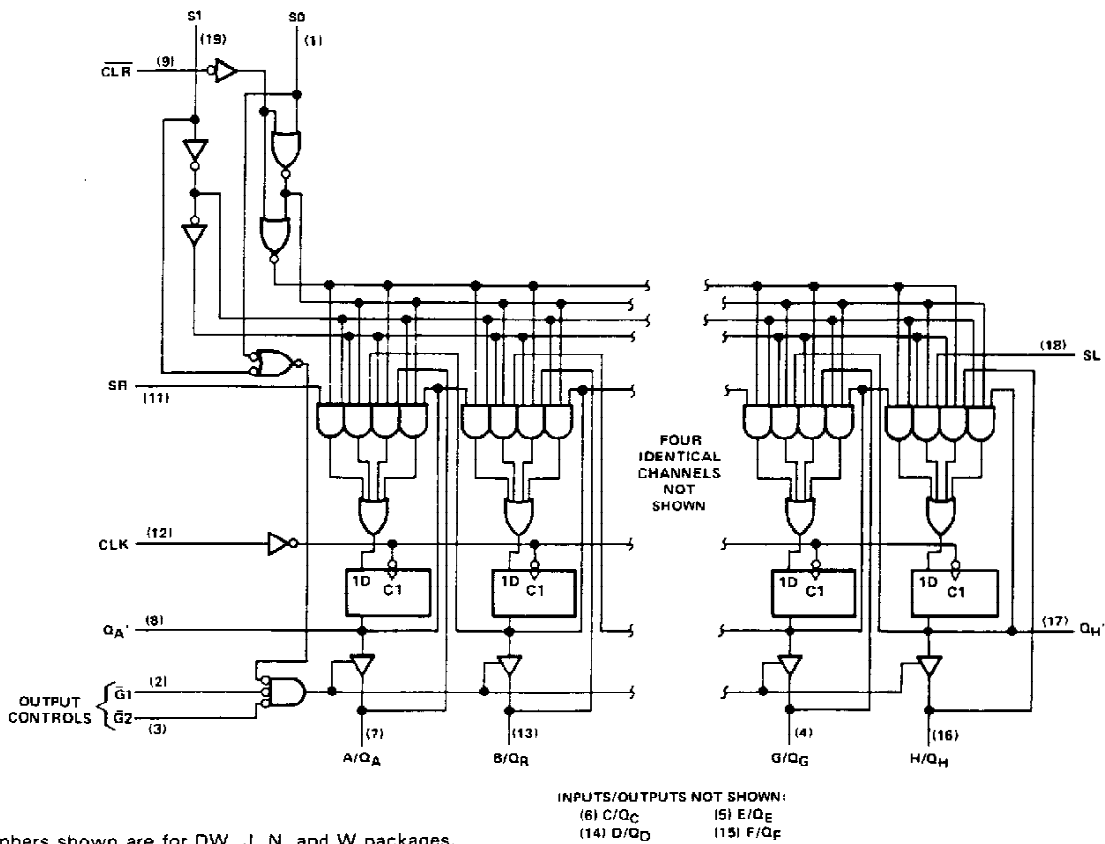
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logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, N, and W packages.

logic diagram (positive logic)



Pin numbers shown are for DW, J, N, and W packages.

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## SN54LS323, SN74LS323 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

schematics of inputs and outputs, absolute maximum ratings, recommended operating conditions, and electrical characteristics

Same as SN54LS299 and SN74LS299, except  $t_{SU}$  (Clear Inactive) does not apply.

switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{max}$			See Note 1	25	35		MHz
$t_{PLH}$	CLK	$Q_A'$ or $Q_H'$	$C_L = 15\text{ pF}$ , $R_L = 2\text{ k}\Omega$		22	33	ns
$t_{PHL}$					26	39	
$t_{PLH}$	CLK	$Q_A$ thru $Q_H$	$C_L = 45\text{ pF}$ , $R_L = 665\ \Omega$		17	25	ns
$t_{PHL}$					25	39	
$t_{PZH}$	$\bar{G}1, \bar{G}2$	$Q_A$ thru $Q_H$	$C_L = 45\text{ pF}$ , $R_L = 665\ \Omega$		14	21	ns
$t_{PZL}$					20	30	
$t_{PHZ}$	$\bar{G}1, \bar{G}2$	$Q_A$ thru $Q_H$	$C_L = 5\text{ pF}$ , $R_L = 665\ \Omega$		10	20	ns
$t_{PLZ}$					10	15	

† $f_{max}$  = maximum clock frequency

$t_{PLH}$  = Propagation delay time, low-to-high-level output

$t_{PHL}$  = Propagation delay time, high-to-low-level output

$t_{PZH}$  = Output enable time to high level

$t_{PZL}$  = Output enable time to low level

$t_{PHZ}$  = Output disable time from high level

$t_{PLZ}$  = Output disable time from low level

NOTE 1: For testing  $f_{max}$ , all outputs are loaded simultaneously, each with  $C_L$  and  $R_L$  as specified for the propagation times. Load circuits and voltage waveforms are shown in Section 1.

  
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